REMARKS

Claims 1-14 are pending in the present application. Claims 1-14 stand rejected. Claim 1, 13, and 14 have been amended. Reconsideration of the claim rejections are respectfully requested in view of the following remarks.

Claim Objections

The Examiner states (in p. 2 of the FINAL ACTION) that claims 1, 13, and 14 are objected to because "property" is not clearly described in the disclosure and in claims 1, 13, and 14. Applicants respectfully disagree. The term "property" as used in the claims should be construed with its ordinary and customary meaning, where "property" generally refers to a trait, attribute, characteristic, quality or distinctive feature of something. Claims 1, 13, and 14 essentially recite "*determining a structural metric from a property of the network graph.*" Page 12, lines 21-22 of the disclosure states that "*[t]he metric is based on the connectivity of the network graph implementing the logic function.*" Since connectivity is clearly a property of the network graph, the term "property" finds clear support in the disclosure. In any event, in the interests of cooperation, claims 1, 13, and 14 have been amended to delete the term "property".

The Examiner further states (in p.2 of the FINAL ACTION) that claims 1, 13, and 14 are objected to because "network graph" is not defined in claims 1, 13 and 14. Applicants disagree. The term "network graph" is a well known term of art, with clear meaning to those skilled in the art. In addition, the term "network graph" is described in the claims as being determined from a logical representation of a circuit design. Further, applicant's disclosure describes network graphs (in p. 14, lines 4-6) by stating that *"[t]he design is first represented as a graph with the circuits represented as nodes and*

connections between them represented as edges", and even illustrates network graphs in figures 6a-6c.

Accordingly, for at least the foregoing reasons, it is respectfully submitted that the objections be withdrawn.

Claim Rejections - § 102

Claims 1-14 stand rejected under 35 U.S.C 102(e) as being anticipated by Gupta (U.S. Pub. 2004/0068711). It is respectfully submitted that, at the very least, Gupta does not anticipate claims 1, 13, and 14.

By way of example, with respect to claims 1, 13 and 14, it is submitted that Gupta does not disclose or suggest, *during logical synthesis of a circuit design, generating a network graph from a logical representation of the circuit design.*

The Examiner states (in p. 2-3 of the FINAL ACTION) that Gupta teaches during logical synthesis, generation of a network graph from a logical representation of the circuit design. Applicants respectfully disagree for the following reasons.

Gupta is **not** concerned with logical synthesis, but with register transfer level (RTL) generation (see FIG. 1), a step that precedes logical synthesis. Applicant's specification states (in p. 2, lines 2-21) that *[l]ogical synthesis comprises two optimization stages: (1) a technology independent stage and (2) a technology dependent stage* and (in p. 3, lines 5-6) that *[t]he technology independent stage comprises transforming a register transfer level textual description of the design into a set of boolean equations.* This means that the register transfer level textual description (RTL) has already been created in a stage of design that **precedes** logical synthesis, because the RTL must first exist in order for logical synthesis to operate on the RTL in the logical synthesis' technology independent

stage. Since Gupta teaches (in FIG. 1, element 116) register transfer level (RTL) generation as a **final result**, clearly Gupta is concerned with processing that occurs **before** logical synthesis. Therefore, it follows that Gupta **cannot** teach generation of a network graph **during** logical synthesis. It should also be noted that applicant's had raised this issue in the response to the NON-FINAL ACTION. The Examiner has failed to respond, which only further supports applicant's position that Gupta does not disclose or suggest *during logical synthesis of a circuit design, generating a network graph from a logical representation of the circuit design.*

Accordingly, at least for the foregoing reasons, claims 1, 13, and 14 and believed to be patentable over Gupta. Moreover, claims 2-12 are believed patentable at least by virtue of their dependence from claim 1.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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